11-26-01

Express Mail Number: EL896635115US

Docket No. B-4392 619330-6
Date: November 16, 2001

A

Commissioner of Patents and Trademarks
Box New Patent Application
Washington, D.C. 20231

Sir:

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): (1) Ta-Lee YU
(2) Shi-Tron LIN

NOTE: Patent must be applied for in the name of all of the actual inventor or inventors.

For: "ESD PROTECTION CIRCUIT TRIGGERED BY LOW VOLTAGE"

Enclosed are:

1. **The Papers Required For Filing Date Under 37 CFR 1.53(b):**

8 Pages of specification 1 Page of abstract 4 Pages of claims

5 Sheets of drawings [X] formal [ ] informal
(Figs. 1, 2A-2C, 3)

[X] In addition to the above papers there is also attached

Postcard
Check for filing fee in the amount of $740.00
Declaration/Power of Attorney (4 pages)
Claim to Priority (1 Page)
Assignment Cover Sheet (1 page), Assignment document (1 page), and Check for $40.00

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this paper and the documents referred to as enclosed therein are being deposited with the United States Postal Service in an Express Mail envelope with sufficient postage for Express Mailing on this date November 16, 2001 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EL896635115US addressed to the:

Commissioner of Patents and Trademarks
Box New Patent Application
Washington, D.C. 20231

Cheryl Liang
(Typed or printed name of person mailing paper)

(Signature of person mailing paper)

NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 CFR 1.10(b).

2. Declaration or oath

[X] Enclosed

[ ] original [X] facsimile

executed by:

[X] inventor(s)

[ ] legal representative of inventor(s) 37 CFR 1.42 or 1.43

[ ] joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached. 37 CFR 1.47.

[ ] petition and statement required by 37 CFR 1.47 also attached. See item 7 below for fee.

[ ] Not Enclosed

[ ] Application is made by a person authorized under 37 CFR 1.41(c) on behalf of all of the above named inventor(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently.

[ ] Showing that the filing is authorized. (Not required unless called into question. 37 CFR 1.41(d)).

NOTE: Where the filing is a completion in the U.S. of an international application under 35 U.S.C. 371(c)(4) then the declaration must be filed.

3. Assignment

[X] An assignment of the invention to

Winbond Electronics Corp.
(with separate cover sheet and separate check for $40.00)

4. Certified Copy

[ ] A certified copy of Application

from which priority is claimed.

NOTE: Must be referred to in oath or declaration. 37 CFR 1.55 and 163.

5. Fee Calculation

CLAIMS AS FILED				
Number Filed		**Number Extra**	**Rate**	**Basic Fee $ 740.00**
Total Claims	18-20=	0 x	$ 18.00	0
Independent Claims	2-3=	0 x	$ 84.00	0
Multiple Dependent Claim(s), If Any		0 x	$ 280.00	0

[ ] Amendment canceling extra claims enclosed

[ ] Amendment deleting multiple dependencies enclosed

[ ] Fee for extra claims is not being paid at this time

NOTE: If the fee for extra claims are not paid on filing they must be paid or the claims canceled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency, 37 CFR 1.16(d).

Filing Fee Calculation $ 740.00

6. **Small Entity Statement**

[ ] Verified statement that this is a filing by a small entity under 37 CFR 1.9 and 1.27.

Filing Fee Calculation (50% of above) $_____

NOTE: If a verified statement is filed within 2 months of the date of payment of first fee then the excess fee paid will be refunded on request. Notice of January 20, 1983. 1027 TMOG 114.

7. **Fee Payment Being Made At This Time**

[ ] Not Enclosed

[ ] No filing fee is submitted. This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.

NOTE: Where the filing is a completion in the U.S. of an international application the fee must be paid.

[X] Enclosed

[X] filing fee $ 740.00

[ ] recording assignment ($40.00; 37 CFR 1.21(h)(i)) $_____

[ ] petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached. 37 CFR 1.47 and 1.17 (h) $_____

Total fees enclosed $ 740.00

8. **Method of Payment of Fees**

[X] check in the amount of $ 740.00

[ ] charge account No. 12-0415 in the amount of $_____
A duplicate of this transmittal is attached.

NOTE: Fees should be itemized is such a manner that it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

9. **Authorization to Charge Additional fees**

[X] The Commissioner is hereby authorized to charge the following additional fees which may be required to Account No. 12-0415:

[X] 37 CFR 1.16 (filing fees and presentation of extra claims)

[X] 37 CFR 1.17 (application processing fees)

[ ] 37 CFR 1.18 (issue fee at or before Mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b))

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application...prior to paying... issue fee".

10. **Instructions As To Overpayment**

[X] Credit Account No. 12-0415 [ ] refund

c/o LADAS & PARRY
5670 Wilshire Boulevard
Suite 2100
Los Angeles, California 90036-5679

Telephone: (323) 934-2300
Telefax: (323) 934-0202

Ross A. Schmitt
Attorney
Reg. No. 42,529

Client's ref.:88-003/2001-11-16
File:0492-4762USF/Hui

EL896635115US

TITLE

ESD PROTECTION CIRCUIT TRIGGERED BY LOW VOLTAGE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a electrostatic discharge (ESD) protection circuit triggered by low voltage. Particularly, the present invention relates to an ESD protection circuit comprising a durable metal oxide semiconductor (MOS).

Description of the Related Art

ESD is a major concern for estimating the reliability of an integrated circuit (IC). All components of the IC having external connections, such as input pins, output pins, I/O pins, and power-bus pins must have the capability to discharge ESD stress and protect the core circuit of the IC.

Referring to Fig.1, the conventional ESD protection circuit in US patent no.5,456,189 uses a lateral semiconductor control rectifier (LSCR) and a MOS transistor to achieve ESD protection. As shown in Fig.1, the ESD protection circuit comprises a p-substrate 16, an N-well 18, a p-type doped region 20 in the N-well 18 as an anode, and an NMOS 22. The NMOS 22 comprises a gate 26, an n-type second doped region 30 and an n-type first doped region 28. The anode 20, the N-well 18, the P-substrate 16 and the second doped region 30 form the LSCR. The first doped region 28 is formed at the junction between the N-well 18 and the P-substrate 16 to dissipate the current in the N-well 18. A p+ first contact region 34 and an n+ second contact region 36 are respectively formed in the P-substrate 16 and the N-well 18 as shown in Fig.1. The second contact

region 36 and the anode 20 are both coupled to a pad 12, then coupled to a core circuit. The gate 26 of the MOS 22 and the first contact region 34 are coupled to a power pad, such as Vss.

When ESD stress occurs at the pad 12, the major voltage drop occurs at the junction between the N-well 18 and the P-substrate 16. Due to the difference of doped concentration between the N-well 18 and the P-substrate 16, an avalanche breakdown voltage is lowest at the junction thereof to allow the current to dissipate into the substrate 16, triggering the LSCR. The ESD stress is discharged through the LSCR and thus the core circuit is protected.

The resistance of the source and drain of the MOS have reduced with the development of the self-aligned-silicide (Salicide) process. A large voltage drop occurs between the first doped region 28 and the gate 26 because of the smaller resistance of the first doped region 28. The gate oxide under the gate 26 is designed to tolerate only low voltages (about 3V) under normal conditions, not the high voltage stress resulting here. A conventional solution is to have the salicide process performed at the core circuit, but not at the ESD protection circuit. By doing so, a photo mask, creating extra manufacturing costs, is needed.

Another solution is to increase the resistance of the first doped region 28 by increasing the length of the first doped region 28. Unfortunately, additional increases in manufacturing costs also result from the increased area of the first doped region 28. Worst of all, the resistance between the first doped region 28 and the MOS is not evenly distributed, causing uneven loading on the MOS gate which then damages the gate oxide of the gate 26.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an ESD protection circuit comprising a durable MOS transistor. The first doped region of the MOS transistor is specially designed to have higher resistance without changing the manufacturing process. Furthermore, the current load on the MOS gate is equally distributed to prevent damage to the gate oxide layer of the MOS gate in an ESD event.

The present invention provides a low-voltage-triggered electrostatic discharge (LVTESD) protection circuit coupled to a pad of an integrated circuit (IC) to protect core circuits of the IC from ESD event. The ESD protection circuit comprises a semiconductor substrate having the first conductivity type, a well region having the second conductivity type formed in the semiconductor substrate, and an anode-doped region having the first conductivity type formed in the well region to become an anode of a semiconductor control rectifier (SCR). The MOS transistor has a gate structure in the semiconductor substrate outside the well region. The gate structure has a first side and a second side. A first doped region having the second conductivity type is formed between the well region and the gate structure immediately adjacent to the first side of the gate structure in the semiconductor substrate. A second doped region having the second conductivity type is formed next to the second side of the gate structure in the semiconductor substrate. A plurality of isolated islands are formed and distributed in the first doped region so that a current flow in the first doped region has to go around the isolated islands and the resistance of the first doped region is increased.

With reference to circuit design, the present invention provides another low-voltage-triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit (IC) to protect the core circuit of the IC from ESD stress. The LVTESD protection circuit comprises a

semiconductor control rectifier (SCR) and a metal oxide semiconductor (MOS). The SCR comprises an anode, a anode gate, a cathode and a cathode gate. The anode is coupled to the pad. The MOS transistor has a second conductivity type and is formed on a semiconductor substrate having a first conductivity type comprising a well having the second conductivity type. The MOS transistor comprises a gate structure, a first doped region and second doped region.

The gate structure is formed on the semiconductor substrate and has a first side and a second side. The first doped region is formed in the semiconductor substrate between the well and the gate structure and is immediately adjacent to the first side of the gate structure. The gate structure comprises at least one contact region coupled to the anode gate. The second doped region is formed in the semiconductor substrate adjacent to the second side of the gate structure, and is coupled to the cathode. A plurality of isolated islands is formed between the contact region and the first side of the gate structure in the first doped region. Current in the first doped region must flow around the isolated islands, increasing the resistance of the first doped region.

The isolated islands can be formed in various ways, mainly to make the current in the first doped region flow around the isolated islands and increase the length of the current path. A field oxide, or a floating gate with an oxide layer and a polysilicon layer, is used to form the isolated islands in the present invention. It is well known that a field oxide can be formed by LOCOS isolation process or by a trench isolation process. Preferably, each of the isolated islands has an elongated profile and is approximately parallel or perpendicular to the first side of the gate structure so that the resistance in the first doped region is increased.

The advantage of the present invention lies in the increased resistance of the first doped region without any change made in the manufacturing process, while the current load received by the MOS gate is distributed to protect the gate oxide of the MOS transistor from ESD stress.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

Fig. 1 is a perspective diagram of a conventional ESD protection circuit;

Fig. 2A is a cross section of the ESD protection circuit of the present invention;

Fig. 2B is a top view of Fig. 2A;

Fig. 2C shows the equivalent circuit diagram of Fig. 2A; and

Fig. 3 shows a cross section of the ESD protection circuit of the other embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The ESD protection circuit of the present invention comprises a durable MOS transistor. A first doped region of the second conductivity type of the MOS transistor is specially designed with higher resistance to protect the gate oxide of the MOS from an ESD event.

As an example of the present invention, the first conductivity type is a p type and the second conductivity type is an n type in the present embodiment. It is apparent to those in the art that the polarity may be exchanged.

Fig. 2A is a cross section of the ESD protection circuit of the present invention, and Figs. 2B and 2C are respectively

the top view and the equivalent circuit diagram of Fig.2A. The ESD protection circuit 10 of the present invention is coupled to a pad 12 of an integrated circuit (IC) to protect the core circuit 14 of the IC from ESD event. The ESD protection circuit 10 comprises a p-type semiconductor substrate 16, an n-well 18 and a p-type anode doped region 20. The n-well 18 is formed in the semiconductor substrate 16. The anode doped region 20 is formed in the n-well 18. A gate structure 22 is formed in the substrate 16 outside the n-well 18 and is comprised of a first side 26 and a second side 24. An n-type first doped region 28 is formed between the n-well 18 and the gate structure 22 and is adjacent to the first side 26 of the gate structure 22 in the semiconductor substrate 16. An n-type second doped region 30 is formed in the semiconductor substrate 16 and adjacent to the second side 24 of the gate structure 22 in the semiconductor substrate 16. A p-type first contact region 34 and an n-type second contact region 36 are respectively formed in the semiconductor substrate 16 and the n-well 18. As shown in Fig.2A, the anode doped region 20, the n-well 18, the semiconductor substrate 16 and the second doped region 30 form a PNPN structure. Therefore, the anode doped region 20, the n-well 18, the semiconductor substrate 16 and the second doped region 30 are respectively the anode, anode gate, cathode gate and cathode of a semiconductor control rectifier (SCR) formed by the PNPN structure.

A plurality of isolated islands of field oxide layers 32 with approximately the same width are evenly formed and distributed in the first doped region 28 as shown in Figs. 2A and 2B. When a current flows through the first doped region 28, the current does not pass through the field oxide layers 32, but around them, so that the resistance of the first doped region 28 is increased.

The first contact region 34, the second doped region 30 and the gate of the gate structure 22 are coupled to a power pad, such as VSS. The first doped region 28 functions as a resistor due to the result of the field oxide 32 layers. One end of the resistor is coupled to the gate structure 22, and the other end is coupled to the n-well 18, the anode gate. The second contact region 36 and the anode doped region 20 are coupled to the pad 12 (the anode). The equivalent circuit diagram of the electronic connection is shown in Fig.2C.

When electrostatic voltage occurs at the pad 12, the voltage is transmitted to a side of the gate structure 22 slowly due to the obstruction of the isolated islands 32 in the first doped region 28. Therefore, it is possible to trigger the SCR before the voltage of the gate structure side 22 exceeds a critical value damaging the gate oxide by adjusting the resistance formed by the isolated islands 32. The gate oxide of the gate structure 22 is thus protected with the side voltage of the gate structure being reduced.

The isolated islands are distributed in the first doped region 28 to divert the current flow in the first doped region 28 and allow it to evenly reach the side of the gate structure 22. The gate structure 22 then uniformly triggers the SCR to achieve optimum ESD protection.

The isolated islands are primarily used to divert at least a portion of the current flow. Alternatively, a floating gate 40 can be used to replace each of the isolated islands, as shown in Fig.3. The floating gate 40 comprises an oxide layer formed on the semiconductor substrate 16 and a polysilicon layer 44 formed on the oxide layer. Gate patterning is tight in the design rule of semiconductor process. Therefore, an increased number of tinier isolated islands are fabricated and larger resistance in the first doped region 28 results. It is noted that an isolated island can be of an elongated shape which can

be approximately parallel or perpendicular to the first side of the gate structure so that the length of the current path is increased and the resistance in the drain doped region 28 becomes higher.

In comparison to the conventional LVTESD circuit in a salicide process of semiconductor manufacturing, the present invention provides a plurality of isolated islands to increase the resistance of the drain doped region of an MOS. As a result, no extra photo mask is needed. It is noted that since the isolated islands can be fabricated thin and long and configured approximately parallel or perpendicular to the first side of the gate structure 22, not much area is needed to accommodate the isolated islands. The configuration of isolated islands helps the gate structure 22 trigger the SCR of the semiconductor evenly and achieve better performance.

Finally, while the invention has been described by way of example and in terms of the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

Client's ref.:88-003/2001-11-16
File:0492-4762USF/Hui

What Is Claimed Is:

1. A low-voltage-triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit (IC) to protect core circuits of the IC from ESD event, the ESD protection circuit comprising:

a semiconductor substrate having the first conductivity type;

an well region having the second conductivity type, formed in the semiconductor substrate;

an anode doped region having the first conductivity type, formed in the well region;

a gate structure, formed in the semiconductor substrate and outside the well region, the gate structure having a first side and a second side;

a first doped region having the second conductivity type, formed between the well region and the gate structure, immediately adjacent to the first side of the gate structure in the semiconductor substrate;

a second doped region having the second conductivity type, formed next to the second side of the gate structure in the semiconductor substrate; and

a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased.

2. The ESD protection circuit in claim 1, wherein the ESD protection circuit further comprises:

a first contact region having the first conductivity type, formed in the semiconductor substrate; and

a second contact region having the second conductivity type, formed in the well region;

wherein the first contact region is coupled to the second doped region and a power pad of the IC, and the anode doped region is coupled to the pad.

3. The ESD protection circuit in claim 1, wherein the second contact region is coupled to the anode doped region.

4. The ESD protection circuit in claim 1, wherein the gate structure has an oxide layer formed on the semiconductor substrate, and a polysilicon layer formed on the oxide layer.

5. The ESD protection circuit in claim 4, wherein the polysilicon layer is coupled to the second doped region.

6. The ESD protection circuit in claim 1, wherein each of the isolated islands comprises an oxide layer formed on the semiconductor substrate, and a polysioicon layer formed on the oxide layer.

7. The ESD protection circuit in claim 1, wherein the isolated islands are field oxide.

8. The ESD protection circuit in claim 1, wherein each of the isolated islands has approximately the same width.

9. The ESD protection circuit of claim 1, wherein each of the isolated islands is elongated and approximately parallel to the first side of the gate structure.

10. The ESD protection circuit of claim 1, wherein each of the isolated islands is elongated and approximately perpendicular to the first side of the gate structure.

11. THE ESD protection circuit in claim 1, wherein the first type is a P-type, and the second conductivity type is an n-type.

12. A low-voltage-triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit (IC) to protect the core circuit of the IC from ESD stress, the LVTESD protection circuit comprising:

a semiconductor control rectifier, comprising an anode, a anode gate, a cathode and a cathode gate, the anode is coupled to the pad; and

a metal-oxide-semiconductor (MOS) having a second conductivity type, formed on a semiconductor substrate having a first conductivity type comprising a well having the second conductivity type, the MOS comprising:

a gate structure, formed on the semiconductor substrate, having a first side and a second side;

a first doped region, formed in the semiconductor substrate between the well and the gate structure and immediately adjacent to the first side of the gate structure, comprising at least one contact region coupled to the anode gate;

a second doped region, formed in the semiconductor substrate adjacent to the second side of the gate structure, and coupled to the cathode; and

a plurality of isolated islands, formed between the contact region and the first side of the gate structure in the first doped region, resulting in increased resistance of the first doped region.

13. The ESD protection circuit in claim 12, wherein each of the isolated islands comprises an oxide layer on the

semiconductor substrate, and a polysilicon layer on the oxide layer.

14. The ESD protection circuit in claim 12, wherein the IC further comprises a plurality of oxide layers, and each of the isolated islands is formed by one of the oxide layers.

15. The ESD protection circuit in claim 12, wherein each of the isolated islands has approximately the same length.

16. The ESD protection circuit in claim 12, wherein each of the isolated islands has an elongated profile and is approximately parallel to the first side of the gate structure.

17. The ESD protection circuit in claim 12, wherein each of the isolated islands has an elongated profile and is approximately perpendicular to the first side of the gate structure.

18. The ESD protection circuit in claim 12, wherein the first conductivity type is a p type, and the second conductivity type is an n type.

ABSTRACT OF THE DISCLOSURE

The present invention provides a low-voltage-triggered electrostatic discharge (LVTESD) protection circuit coupled to a pad of an integrated circuit (IC) to protect core circuits of the IC from ESD. The ESD protection circuit comprises a semiconductor substrate having the first conductivity type, a well region having the second conductivity type is formed in the semiconductor substrate, and an anode-doped region having the first conductivity type and formed in the well region to become an anode of a semiconductor control rectifier (SCR). A gate structure is formed in the semiconductor substrate outside the well region. A first doped region having the second conductivity type is formed between the well region and the gate structure in the semiconductor substrate. A second doped region having the second conductivity type is formed adjacent to the second side of the gate structure in the semiconductor substrate. A plurality of isolated islands are evenly formed and distributed in the first doped region so that current in the first doped region must flow around the isolated islands to increase the resistance of the first doped region.

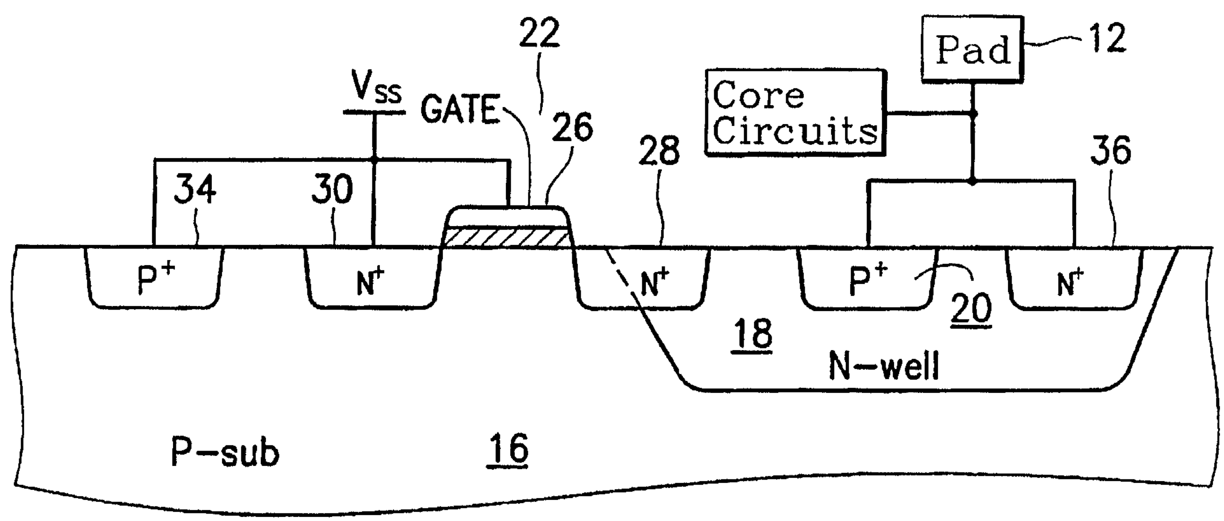
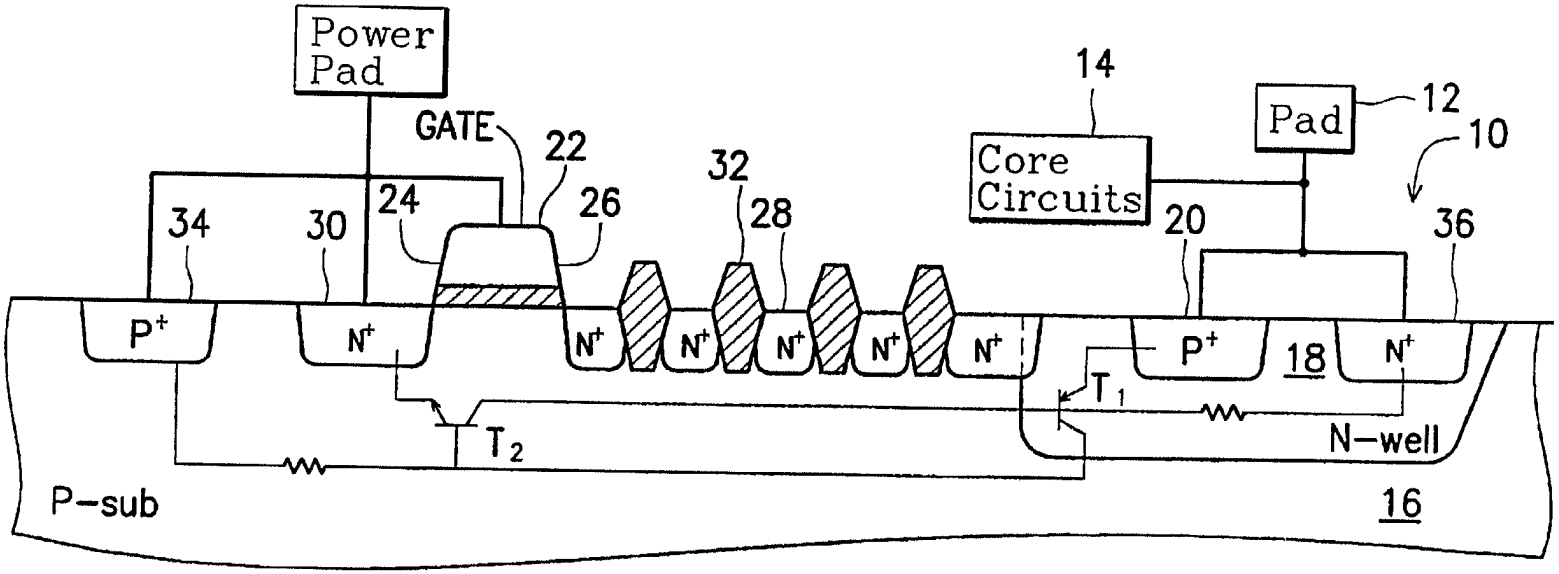


FIG. 1 (PRIOR ART)


Power Pad
GATE
22
24
26
32
28
34
30
14
Core Circuits
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12
10
20
36
P+
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T2
N-well
P-sub
16

FIG. 2A

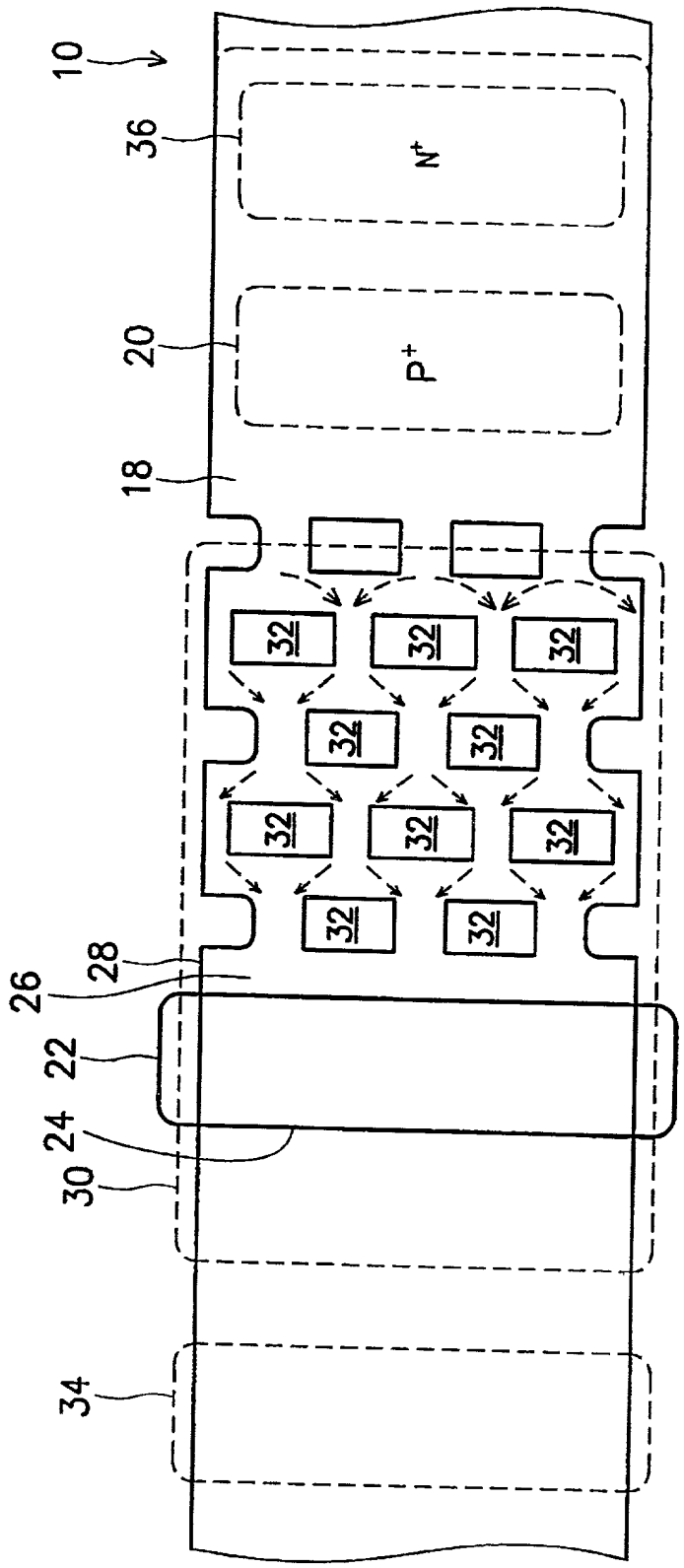

FIG. 2B

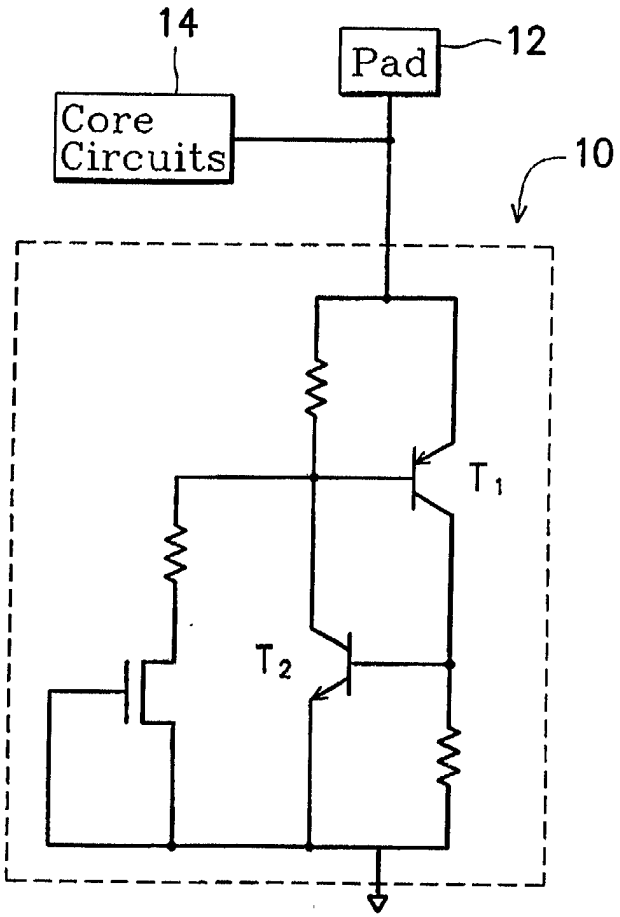

FIG. 2C

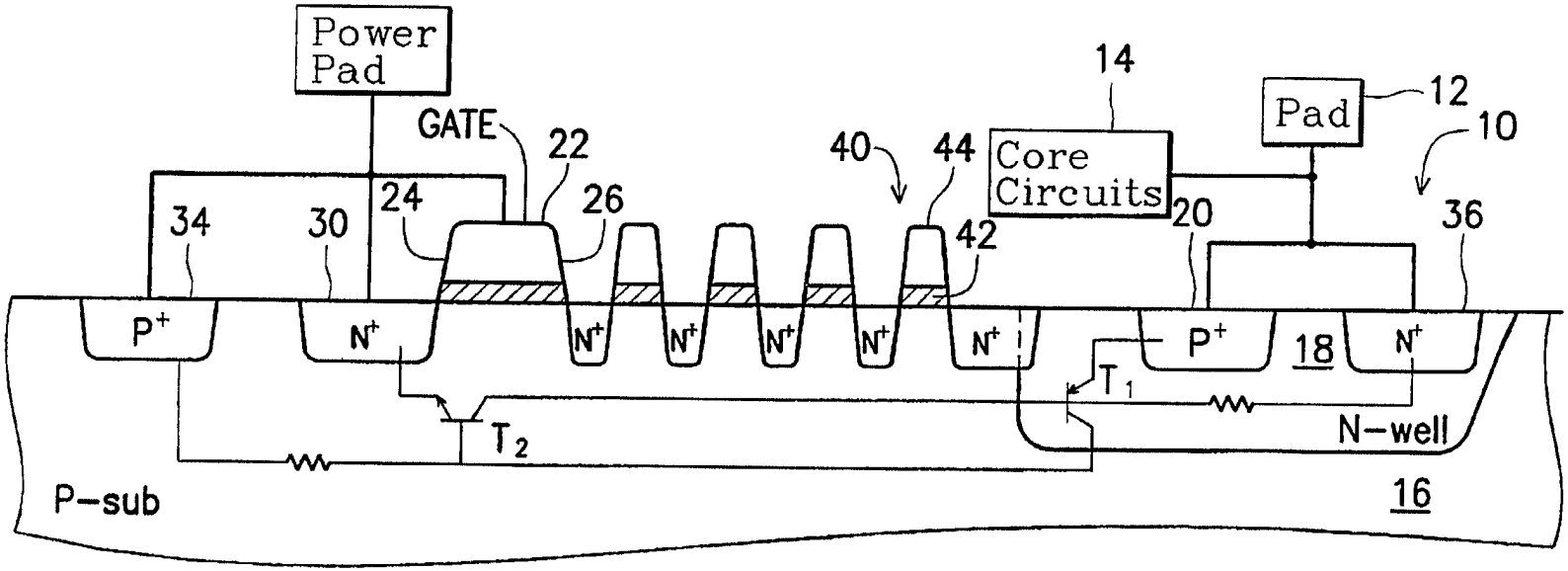

FIG. 3

PATENT Attorney's Docket No. B-4392 619330-6

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR CIP)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: *(check one applicable item below)*

[x] original
[ ] design
[ ] supplemental

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application, do not check next item; check appropriate one of last three items.

[ ] national stage of PCT

NOTE: If one of the following 3 items apply, then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION, OR CIP.

[ ] divisional
[ ] continuation
[ ] continuation-in-part (CIP)

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

ESD PROTECTION CIRCUIT TRIGGERED BY LOW VOLTAGE

SPECIFICATION IDENTIFICATION

the specification of which: *(complete (a), (b) or (c))*

(a) [x] is attached hereto.
(b) [ ] was filed on _____ as [ ] Serial No. / ____
or [ ] Express Mail No., *as Serial No. not yet known,* _____
and was amended on ____ *(if applicable).*

NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) [ ] was described and claimed in PCT International Application No. _____
filed on _____ as amended under PCT Article 19 (1)
on _____ *(if any).*

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code Federal Regulations § 1.56.

[ ] In compliance with this duty there is attached an information disclosure statement 37 CFR 1.97.

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign applications(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) [ ] no such applications have been filed.
(e) [X] such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. claimed priority check item (e), enter the details below and make the priority claim.

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN(S)) PRIOR TO THIS U.S. APPLICATION

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119 [ ] YES [ ] NO
Taiwan, R.O.C.	89124513	20/11/2000	[X] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN(S)) PRIOR TO THIS U.S. APPLICATION

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(List name and registration number)*

Richard P. Berg, Reg. No. 28,145
Mavis S. Gallenson, Reg. No. 32,464
Kam C. Louie, Reg. No. 33,008
Ross A. Schmitt, Reg. No. 42,528
Victor Repkin, Reg. No. 45,039
John Palmer, Reg. No. 38,885
Peter D. Galloway, Reg. No. 27, 885
William R. Evans, Reg. No. 25, 858

(check the following item, if applicable)

[ ] Attached as part of this declaration and power of attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO:
Richard P. Berg, Esq.
c/o LADAS & PARRY
5670 Wilshire Boulevard, Suite 2100
Los Angeles, California 90036-5679

DIRECT TELEPHONE CALLS TO: *(Name and telephone number)*

Richard P. Berg

(323) 934-2300

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE

Full name of **first** inventor Ta-Lee YU

Inventor's signature Ta-Lee Yu

Date Nov. 15, 2001 Country of Citizenship Taiwan, R.O.C.

Residence Same as the Post Office Address (below)

Post Office Address 4F, No. 1, Alley 40, Lane 572, Sec. 4, Chung-Hsing Rd., Chutung Chen, Hsinchu Hsien, Taiwan, R.O.C.

Full name of **second** inventor Shi-Tron LIN

Inventor's signature Shi-Tron Lin

Date Nov. 16, 2001 Country of Citizenship U.S.A.

Residence Same as the Post Office Address (below)

Post Office Address 9F, No. 69, Sec. 2, Yen-Ping N. Rd., Lin 15, Chao-Yang Li, Ta-Tung District, Taipei, Taiwan, R.O.C.

CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGES(S) WHICH FORM A PART OF THIS DECLARATION

[ ] Signature for third and subsequent joint inventors. *Number of pages added*

[ ] Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _

[ ] Signature for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. *Number of pages added Added* pages to combined declaration and power of attorney for divisional, continuation-in-part (CIP) application.
Number of pages added __

[ ] Authorization of attorney(s) to accept and follow instructions from representative.

If no further pages form a part of this Declaration then end this Declaration with this page and check the following item.

[X] This declaration ends with this page.

TOTAL P.06